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09/652,694	08/31/2000	Paul S. Gyskiewicz	INTL-0447-US (P9445)	3816

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EXAMINER
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YENKE, BRIAN P

ART UNIT	PAPER NUMBER
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2614

70

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/652,694

Applicant(s)

GRYSKIEWICZ, PAUL S.

Examiner

BRIAN P. YENKE

Art Unit

2614

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Appeal Brief 23 September 03.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. The examiner has withdrawn the previous Final Rejection (paper 5) in lieu of the Applicant's Appeal Brief filed 23 September 2003, any inconvenience is regretted. The examiner is making the current rejection a Final Rejection being necessitated from applicant's amendment on 31 March 2003.

#### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,4 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Auld et al., US 6,556,193.

In considering claims 1 and 16,

*a) the claimed scaling a first portion and a second portion of image information to provide a scaled first portion and a scaled second portion, wherein unscaled said first portion would substantially fill a first memory area is met where Auld discloses a system where a display can show multiple pictures (PIP's) if desired where the frame buffer is used to store an original image (wherein unscaled the original (first portion) would fill the frame buffer) and where the user selects another image(s) (i.e. PIP), the scaled first and*

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other(s) images would be stored in the same frame buffer (Fig 17a/b), where the frame buffer may include results from other scaling and/or deinterlacing operations (col 18, line 44-67).

*b) the claimed storing said scaled first portion and said scaled second portion in said first memory area* is met where the scaled first and other(s) images would be stored in the frame buffer (Fig 17a/b), where the frame buffer may include results from other scaling and/or deinterlacing operations (col 18, line 44-67).

In considering claim 4,

*a) the claimed a memory comprising a number of bytes* is met by the frame buffer/memory buffer 240.

*b) the claimed a scaler to perform a scaling operation* is met by horizontal and vertical scaler steps (steps 1712, 1714 Fig 17a); where the frame buffer is used to store an original image (wherein unscaled would fill the frame buffer) and where the user selects another image(s), the scaled first and other(s) images would be stored in the frame buffer (Fig 17a/b), where the frame buffer may include results from other scaling and/or deinterlacing operations (col 18, line 44-67).

*c) the claimed a memory controller...* is met by graphics processor 210 (Fig 2).

The examiner also notes given the broadest interpretation of the independent claims, any display which is able to display a main image with the option of an additional image (PIP, split-screen, dual screen) where the image(s) are stored in a frame buffer

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(memory) before being displayed, will anticipate the independent claims as stated in the rejection above.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh et al., US 6,411,334 in view of applicant's admitted prior art (AAPA) and Michelson, US 5,406,311.

In considering claims 1 and 16,

a) *the claimed scaling a first portion and a second portion of image information to provide a scaled first portion and a scaled second portion...* is met where filtering unit 330, which horizontally scales/filters (332/334) and vertically scales/filters (336/338) where memory buffer 240 stores the temporary data in properly sized buffers (col 4, line 6-8). Thus the unscaled portion if stored in a properly sized buffer would substantially fill a memory area.

However, Yeh does not specifically disclose storing the scaled first portion and scaled second portion in the first memory area, where the unscaled portion would fill the first memory area.

Yeh discloses an aspect ratio correction using digital filtering which scales a source array of pixel data in a memory by a scale factor to a destination array of pixel data. Again, Yeh does disclose storing the temporary data in properly sized buffers.

It is also known that if data is scaled down (i.e. 2 to 1), only half of the original pixel information would be retained, thus reducing the size of the memory row used (as shown in AAPA drawings Fig 4b-c).

Thus the question of obviousness is whether Yeh which discloses scaling a source array of pixel data (both in the horizontal and vertical directions) into a destination array of pixel data where properly sized buffers are used, where it is known (AAPA) that if a reduction operation is performed only a portion of the original memory row would be used, the examiner maintains it would have been obvious for the following reasons.

It is conventional in the art to utilize the entire row of memory in order to overcome the wasting/non-use of memory. The examiner incorporates Michelson, US 5,406,311 which discloses storing a digitized stream of interlaced video into a memory in non-interlace form. Michelson discloses that the length of the horizontal line is shorter than the page width where Michelson overcomes the wasting of any memory space/rows by writing the horizontal lines and portions of the horizontal lines, by filling the page rows of the memory (Fig 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yeh and AAPA, which discloses scaling data both horizontally and vertically, by storing the scaled horizontal (first portion) and scaled vertical portion (second portion) in the first memory area by using properly sized buffers, with Michelson, by using the entire row of memory, in the event a source of pixel data is reduced from it's original size, to eliminate any waste of memory space/rows.

In considering claims 2 and 17,

*a) the claimed accessing the first or second portion...* is met by graphics processor 210 of display processor 180 (Fig 2) which receives scaled data both from memory 240 and via pre-processing unit 320 (via memory interface 220).

*b) the claimed retrieving a data sample...* is met by filtering unit 330 which receives coefficients from memory buffer 240 and pixel data from pre-processing unit 320 (via memory interface 220).

*c) the claimed using the data sample in a second scaling operation* is met where the data is first scaled horizontally then vertically (Fig 3b).

In considering claims 3 and 18,

*a) the claimed dividing a memory into a plurality of lines* is met by graphics processor 210, which scales the array to a desired destination array of pixel data.

*b) the claimed identifying a line* is met by graphics processor 210 (Fig 3a)

*c) the claimed storing a number of scaled portions in the line...* is met by graphics processor 210 which stores the scaled portions (using filtering unit 330) into memory buffer 240 (Fig 2) .

In considering claims 4-6 and 15,

*a) the claimed a memory...* is met by memory buffer 240

*b) the claimed scaling a first portion and a second portion of image information to provide a scaled first portion and a scaled second portion...* is met where filtering unit 330, which horizontally scales/filters (332/334) and vertically scales/filters (336/338) where memory buffer 240 stores the temporary data in properly sized buffers (col 4, line 6-8). Thus the unscaled portion if stored in a properly sized buffer would substantially fill a memory area.

*c) the claimed a memory controller coupled to the memory* is met by graphics processor 210 (Fig 2).

However, Yeh does not specifically disclose storing the scaled first portion and scaled second portion in the first memory area, where the unscaled portion would fill the first memory area.

Yeh discloses an aspect ratio correction using digital filtering which scales a source array of pixel data in a memory by a scale factor to a destination array of pixel data.



It is also known that if data is scaled down (i.e. 2 to 1), only half of the original pixel information would be retained, thus reducing the size of the memory row used (applicant's drawings Fig 4b-c).

Thus the question of obviousness is whether Yeh which discloses scaling a source array of pixel data (both in the horizontal and vertical directions) into a destination array of pixel data where properly sized buffers are used, where it is known (AAPA) that if a reduction operation is performed only a portion of the original memory row would be used, the examiner maintains it would have been obvious for the following reasons.

It is conventional in the art to utilize the entire row of memory in order to overcome the wasting/non-use of memory. The examiner incorporates Michelson, US 5,406,311 which discloses storing a digitized stream of interlaced video into a memory in non-interlace form. Michelson discloses that the length of the horizontal line is shorter than the page width where Michelson overcomes the wasting of any memory space/rows by writing the horizontal lines and portions of the horizontal lines, by filling the page rows of the memory (Fig 9).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Yeh and AAPA, which discloses scaling data both horizontally and vertically, by storing the scaled horizontal (first portion) and scaled vertical portion (second portion) in the first memory area by using properly sized buffers, with Michelson, by using the entire row of memory, in the event a source of pixel data is reduced from its original size, to eliminate any waste of memory space/rows.

In considering claim 7,

*The claimed wherein the number of bytes in the memory is smaller than the predetermined number of bytes* is met where if the received video data stream is to be displayed on a correspondingly smaller destination display screen (302), the required memory in a decimation operation would be smaller.

In considering claim 8,

*The claimed wherein the scaling operation is a horizontal scaling operation* is met by horizontal filter 1 (332) and horizontal filter 2 (334) Fig 3b.

In considering claims 9-11,

*The claimed wherein a second scaler to perform a second scaling operation* is met by vertical filter 1 (336) and vertical filter 2 (338) which perform a scaling operation on the columns of data.

In considering claims 12-13,

Yeh discloses using digital filtering using horizontal and vertical filters/scalers which correct for an aspect ratio of a display by scaling a source array of pixel data in a memory by a scale factor to a destination array of pixel data.

However, Yeh remains silent on the scalers including a finite impulse response filter (FIR) with a look-up table.

Yeh does disclose that the horizontal coefficients (Fig 4) are processed/loaded into coefficient unit 410 (Fig 4) and the vertical coefficients are processed by vertical coefficient registers 1010-1012 (Fig 10), where the coefficients are both received from memory buffer 240.

A FIR filter is a type of digital filter, which has a finite impulse response, since there is no feedback in the filter. FIR filters are known to be "linear phase", which delay the input signal, but do not distort its phase. In addition, FIR filters are used in interpolation and decimation operations since the FIR filters allow some of the calculations to be omitted, thus providing efficiency in computing operations.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify/utilize a FIR filter, with Yeh, which discloses scaling source array of pixel data in a memory, where the arrays are scaled both horizontally and vertically, by using a FIR filter, in order to provide an efficient linear phase interpolation/decimation operation.

In considering claim 14,

The examiner takes "OFFICIAL NOTICE" in regards to a First-in-First Out Memory. Yeh et al., discloses a memory uses a memory buffer (240), to correct the aspect ratio of a display by scaling the source array of pixel data in memory by a scale factor to a destination array of pixel data.

A FIFO memory, is a conventional device which exits the item/data from the system which has been in the system the longest. Thus data that has arrived

subsequently to previous data, will be exited/output subsequently to the previous data as well.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify/utilize a FIFO memory architecture with Yeh, which discloses the changing/scaling the source array of pixels in a memory, by reading/writing data in and out of the memory in the order the data was received, to thereby maintain the integrity of the original data.

### ***Conclusion***

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Yenke whose telephone number is (703) 305-9871. The examiner work schedule is Monday-Thursday, 0730-1830 hrs.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, John W. Miller, can be reached at (703) 305-4795.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231


**or faxed to:**

**(703) 872-9314**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703)305-HELP.

B.P.Y.

19 February 2004

  
JOHN MILLER  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600